CLAIMS

What is claimed is:

1. An integrated circuit (IC) comprising:

a clock distribution grid distributing a clock to local circuits, said distribution grid having a known load capacitance;

a clock driver driving said clock distribution grid;

at least one inductor connected at one end to said distribution grid, said clock having a frequency within the frequency range of the resonant frequency of local grid capacitance and said at least one connected inductor; and

a power grid, power grid lines being discontinuous in the vicinity of each said at least one inductor, whereby power grid line loops are open in the vicinity of each said at least one inductor.

2. An IC as in claim 1, wherein said at least one inductor is connected to a decoupling capacitor (decap) at an other end.

3. An IC as in claim 2, wherein a voltage develops across each said decap, said voltage being midway between a high level and low level of said clock.

4. An IC as in claim 3, wherein said decap is a pair of decaps, a first of said pair being connected between a first supply line and said other end of said inductor and an other of said pair being connected between said other end and a second supply line.

5. An IC as in claim 4, wherein said second supply line is a ground line.

6. An IC as in claim 1, wherein said power grid lines include supply and supply return lines terminating on endpoints.

7. An IC as in claim 1, wherein said at least one inductor is four inductors located in four quadrants around said clock driver.

8. An integrated circuit (IC) comprising:

a clock distribution grid distributing a clock to local circuits, said distribution grid having a known load capacitance;

a clock driver driving a first clock phase in said clock distribution grid;

at least one inductor connected at one end to said first clock phase, said clock having a frequency within the frequency range of the resonant frequency of local grid capacitance and said at least one connected inductor; and

a second clock phase, said at least one inductor being connected to said second phase at an other end, said local grid capacitance comprising local wiring capacitance from both of said first clock phase and said second clock phase.

9. An IC as in claim 8, further comprising:

a pair of cross coupled inverters connected between said first clock phase and said second clock phase.

10. An IC as in claim 8, further comprising a second clock driver driving said second clock phase.

11. An IC as in claim 8, wherein said at least one inductor is four inductors located in four quadrants around said clock driver.

12. An integrated circuit (IC) assembly clocked by a global clock, said global clock being distributed to a plurality of sectors, each of said sectors comprising:

a clock distribution grid distributing a sector clock to local circuits, said distribution grid having a known load capacitance;

a clock driver driving said clock distribution grid;

at least one inductor connected at one end to said distribution grid, said clock having a frequency within the frequency range of the resonant frequency of local grid capacitance and said at least one connected inductor; and

a power grid, power grid lines being discontinuous in the vicinity of each said at least one inductor, whereby power grid line loops are open in the vicinity of each said at least one inductor.

13. An IC assembly as in claim 12, wherein said at least one inductor is connected to a decoupling capacitor (decap) at an other end.

14. An IC assembly as in claim 13, wherein a voltage develops across each said decap, said voltage being midway between a high level and low of said clock.

15. An IC assembly as in claim 14, wherein said decap is a pair of decaps, a first of said pair being connected between a first supply line and said other end of said inductor and an other of said pair being connected between said other end and a second supply line.

16. An IC assembly as in claim 15, wherein said second supply line is a ground line.

17. An IC assembly as in claim 12, wherein said clock driver is driving a first clock phase, said one end of said at least one inductor being connected to said first clock phase, said IC further comprising:

a second clock phase, said at least one inductor being connected to said second phase at an other end, said local grid capacitance comprising local wiring capacitance from both of said first clock phase and said second clock phase.

18. An IC assembly as in claim 17, further comprising:

a pair of cross coupled inverters connected between said first clock phase and said second clock phase.

19. An IC assembly as in claim 17, further comprising a second clock driver driving said second clock phase.

20. An IC assembly as in claim 12, wherein said at least one inductor is four inductors located in four quadrants around said clock driver.

21. An integrated circuit (IC) assembly clocked by a global clock, said global clock being distributed to a plurality of sectors, each of said sectors comprising:

a clock distribution grid distributing clock phases to local circuits, said distribution grid having a known load capacitance for each of said phases;

a clock driver driving a first phase of said phases; and

at least one inductor connected at one end to said first phase and to said second phase at an other end, said clock having a frequency within the frequency range of the resonant frequency of load capacitance for both of said first phase and said second clock phase and said at least one.

22. An IC assembly as in claim 21, further comprising:

a power grid, power grid lines being discontinuous in the vicinity of each said at least one inductor.

23. An IC assembly as in claim 22, wherein said power grid lines include supply and supply return lines terminating on endpoints, whereby power grid line loops are open in the vicinity of each said at least one inductor.

24. An IC assembly as in claim 21, further comprising:

a pair of cross coupled inverters connected between said first clock phase and said second clock phase.

25. An IC assembly as in claim 24, further comprising a second clock driver driving said second clock phase.

26. An IC assembly as in claim 21, wherein said at least one inductor is four inductors located in four quadrants around said clock driver.

27. An IC assembly as in claim 21, wherein said clock grid is on a first IC chip and ones of said at least one inductor are on an interposer connected to said first chip.